A Multiprocessor DSP System for a High Throughput Control Application

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• Introduction

- Experimental project for research in multiprocessor hardware and software
- Consists of up to six DSPs (TMS320C6000 family)
- The system should also be used to develop a control system for a high precision measurement machine
- high throughput and low latency is a requirement

➤ We need a fast and efficient data transport between the processor nodes!

• Communication structure

- A bus-like communication structure with one master and four slaves
- Master:
  - communicates with the sensors and actors
  - distributes data to the slaves
  - Collects data from the slaves
- Slaves:
  - Runs control algorithms at full speed
  - Accessed via they host port interface(HPI) ➢zero communication overhead
- 'Comm'-processor
  - Communication with the outside world via USB 2.0
  - Manages data compression for a faster transport of large volume data
  - Connected to the master via the HPI of them

See figure 1 ⇨

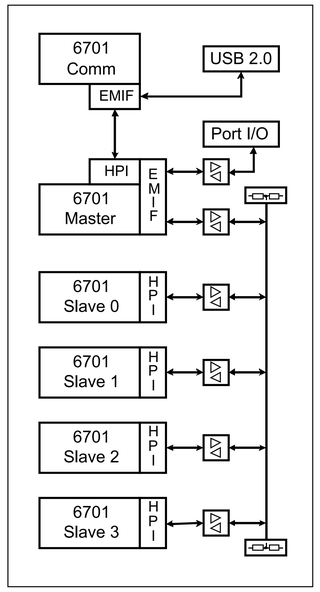

Fig. 1: Overall hardware structure

• Master address ranges

- Slaves appear to the master as memory devices
- Each slave is assigned a memory range (for individual read/write operations)

Surrounding project:

- Some coupled control loops
- They need often the same input data
- Master has to transfer most of the input data to some or all slaves

➢a broadcast ability is recommended

• HPI-broadcast

- Master should write to the HPI of one or all slaves

➢we implemented a special 'broadcast' feature

- It allows the master to write simultaneously into memory locations of all slaves
- Timing of this is virtually equal to normal writes
- Saves time in contrast to access all slaves in sequence

- A dedicated address range is assigned for this feature
- Master can choose one or all slaves by address variation
- A special handling of control signals had to be implemented

• Control logic

- Address decoder generates appropriate chip enable signals for the slaves
- WAIT signal from the slaves must be merged to handle different timing situations

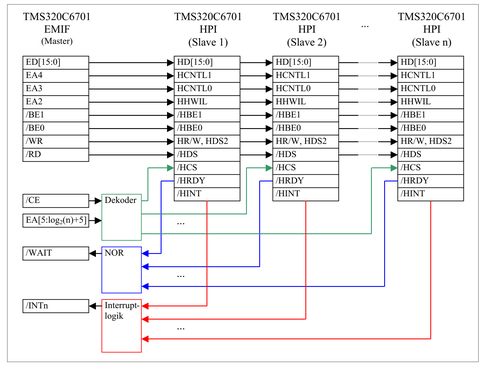

Fig. 2: Control signals (simplified)

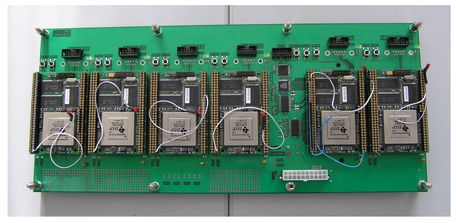

Fig. 3: Board (top view), Modules from right to left: Comm, Master, Slaves 0 - 3

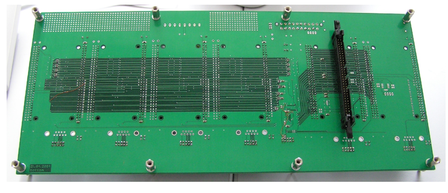

Fig. 4:Board (bottom view)

• Experimental Results

- The timing of the masters bus cycle has been tuned experimental
- At 167 Mhz, a 9-9-3 figure (setup-strobe-hold) has been reached
- Strobe duration is most critical, because WAIT signals must reliably be recognized
- Broadcast mode does not differ from individual access to the slaves (table 1)
- Burst mode provides substantial advantage for large data blocks

Direction and Mode	Data Rate (MByte/s)
Read from slave	6,1
Read from slave (burst)	13,3
Write to slave (burst)	14,5
Broadcast write to slaves (burst)	14,5

Tab. 1: Measured data rates.

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